Application No.: 10/054,241 Docket No. EMC2-078AUS

REMARKS

Reconsideration and re-examination are hereby requested.

Claim 56 has been amended to correct at typographical error.

An IDS was filed electronically on April 19, 2005, copy enclosed. An IDS was filed November 2, 2004, copy enclosed. It does not appear that the Examiner initialed either one of the IDS forms.

Claims 11-16, 19-26, 28-35, and 38-59 stand rejected as being either anticipated or obvious over Hisano et al (U. S. Patent No. 5,241,640.

Before pointing out how the claims distinguish over Hiasno et al., perhaps it might be helpful to review features of applicant's invention.

Referring to FIG. 2 of the patent application, it is noted that "user data" passes through a different communication system than "interface state" data. In the embodiment shown in FIG. 2, the ***interface state data*** passes information ***among the directors*** through a bus system comprising buses BUS A, BUS B, BUS C, and BUS D. The user data, on the other hand, passes through the cache memory 120 through buses 126.

Other features are pointed out below.

Referring to Hiasno et al, at column 3, beginning at line 11:

> The cache memory unit 2 is configured of a cache memory 22 and a directory memory 221. The cache memory 22 is for storing copies of the data stored in the magnetic disk units 4 in a format equivalent to the data in the internal storage of the magnetic disk units 4, for example, in a format including a count section, a key section and a data section. In the cache memory 22, for example, a memory having a width of 16-byte bus is coupled to four 4-byte buffers, each output of which is controlled by a microprocessor or the like.
>
> The directory memory 221 is for controlling, on the basis of the well-known LRU (Least Recently Used) rule, the information on the position where the data in the cache memory 22 is stored within the magnetic disk units 4 (cylinder number or head number), and the information indicating the the addresses corresponding to the storage positions in the cache memory 22. In order to use the cache memory 22 efficiently, the directory memory 221 also controls the storage of new data in the cache memory 22 from the magnetic disk units 4 and the removal of the data already stored in the cache memory 22. (emphasis added)

See also column 6, lines 11-16:

> This operation is realized by searching the directory memory 221 on the basis of the information on the target data storage position (cylinder number and head number) in the magnetic disk units 4 and the like, which information accompanies the command as a parameter arriving from the channel Ch.

First, it is also noted that the claims were amended in the last response to point out that the memory ***has a memory region and that such region has a data port, such data port being coupled to, or in communication with, both the user data port and the interface state data port of a director.*** It is respectfully requested that the Examiner more clearly point out where in Hiasno et al, ***has a memory region and that such region has a data port, such data port being coupled to, or in communication with, both the user data port and the interface state data port of a director.***

Further:

Claim 11 points out that: (1) each one of the directors includes an **interface state data** bus section, for **carrying interface state** data; (2) a plurality of end-user data busses, for **carrying end-user data**; and (3) wherein the central processing units of such plurality of directors control **the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data** generated by **the directors, such generated interface state data being transferred *among* the directors via the interface state data bus section.**
It is respectfully requested that the Examiner point out in Hisano et al., where **such generated interface state data is transferred *among* the directors via the interface state data bus section** .

Claim 20 points out that the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, ***such generated interface state data being transferred among the directors via the interface state data bus***.

It is respectfully requested that the Examiner point out in Hisano et al., where ***such generated interface state data is transferred among the directors via the interface state data bus section***.

Claim 21 points out that: wherein such central processing units of the plurality of directors control the end-user data transfer between the host computer and the bank of disk drives via the end-user data busses in response to interface state data generated by the directors, ***such generated interface state data being transferred among the directors via the interface state data bus section***.

It is respectfully requested that the Examiner point out in Hisano et al., where ***such generated interface state data is transferred among the directors via the interface state data bus section***.

Claim 29 points out: (1) providing an interface state data section for carrying interface state data, **such interface state data section being in communication with the at least one front-end one and the at least one rear-end one of the directors** and the data port of the memory region; (2) providing a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the data port of the memory region; and (3) wherein such central processing units of the plurality of directors control the end-user data transfer between the host computer and the bank of disk drives and the memory via the end-user data busses in response to interface state data generated by the directors, **such generated interface state data being transferred among the directors**.

It is respectfully requested that the Examiner point out in Hisano et al., where **such generated interface state data is transferred among the directors**.

Claim 30 points out that: (1) an interface state data bus section, for carrying interface state data, **such interface state data bus section being in communication with both the front-end portion of the plurality of directors** and the rear end portion of the plurality of directors and the data port of the memory region; (2) plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a

first end coupled to a corresponding one of the plurality of directors and a second end coupled to the data port of the memory region; and (3) wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, **such generated interface state data being transferred among the directors**.

It is respectfully requested that the Examiner point out in Hisano et al., where **such generated interface state data is transferred among the directors.**

Claim 39 points out: (1) providing **an interface state data section for carrying interface state data, such interface state data section being in communication with the front end portion of the directors and the rear end portion of the directors** and the data port of the memory region; (2) providing a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the data port of the memory region; and (3) wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives and the memory via the end-user data busses in response to interface state data generated by the directors, ***such generated interface state data being transferred among the directors***.

It is respectfully requested that the Examiner point out in Hisano et al., where **such generated interface state data is transferred among the directors.**

Claim 40 points out: (1) an interface state data bus section, **for carrying interface state data, such interface state data bus section being in communication with both the front-end portion of the plurality of directors and the rear end portion of the plurality of directors** and the data port of the memory region; (2) a plurality of end-user data busses, for carrying end-user data, each one of a first portion of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of front end directors and a second end coupled to the memory and each one of a second portion of the plurality of end user data buses having a first end coupled to a corresponding one of the plurality of rear end

directors and a second end coupled to the data port of the memory region; and (3) wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, ***such generated interface state data being transferred among the directors***.

It is respectfully requested that the Examiner point out in Hisano et al., where **such generated interface state data is transferred among the directors.**

Claim 44 points out: (1) providing an interface state data section for carrying interface state data, **such interface state data section being in communication with the plurality of front end directors and the plurality of rear end directors** and the data port of the memory region; (2) providing a plurality of end-user data busses, for carrying end-user data, each one of a first portion of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of front end directors and a second end coupled to the memory and each one of a second portion of the plurality of end user buses having a first end coupled to a corresponding one of the plurality of the rear end directors and a second end coupled to the data port of the memory region; (3) wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives and the memory via the end-user data busses in response to interface state data generated by the directors, **such generated interface state data being transferred among the directors.**

It is respectfully requested that the Examiner point out in Hisano et al., where **such generated interface state data is transferred among the directors.**

Claim 48 points out: (1) a plurality of directors, ***each one of the directors having an end user data port and an interface state data port***; and (2) wherein the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing through the interface state data ports of the directors***.

It is respectfully requested that the Examiner point out in Hisano et al., where: ***each***

one of the directors having an end user data port and an interface state data port; and where the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing through the interface state data ports of the directors***.

Claim 49 points out: wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.***

It is respectfully requested that the Examiner point out in Hisano et al., where: the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.***

Claim 50 points out that: (1) each one of the directors having an end user data port and an interface state data port; (2) wherein the directors control end user data transfer with end user data in such end user data transfer passing to the cache memory through the end user data ports in response to ***interface state data passing through the interface state data ports of the directors***.

It is respectfully requested that the Examiner point out in Hisano et al., where: ***interface state data passing through the interface state data ports of the directors***.

Claim 51 points out that: each one of the first directors having an end user data port and an interface state data port; and wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the end user data ports ***in response to interface state data passing between the first director and the second director through the interface state***

data ports of the plurality of first directors and the plurality of second directors.

It is respectfully requested that the Examiner point out in Hisano et al., where *interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors*.

Claim 52 points out: *wherein the data port is coupled to the plurality of directors through the end user data communication channel and through the interface state data communication channel*.

It is respectfully requested that the Examiner point out in Hisano et al., where *the data port is coupled to the plurality of directors through the end user data communication channel and through the interface state data communication channel*.

Claim 53 points out: wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through an *end user communication channel in response to interface state data passing between the first director and the second director through a different, interface state data communication path*; and **wherein the data port is coupled to the plurality of directors through the end user data communication channel and through the interface state data communication channel.**

It is respectfully requested that the Examiner point out in Hisano et al., where an *end user communication channel in response to interface state data passing between the first director and the second director through a different, interface state data communication path*; and **wherein the data port is coupled to the plurality of directors through the end user data communication channel and through the interface state data communication channel.**

Claim 54 points out: each one of the directors **having an end user data port *and* an interface state data port,** *one of such ports being coupled to a crossbar switch;* wherein the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory *in response to interface state data passing through the interface*

state data ports of the directors.

It is respectfully requested that the Examiner point out in Hisano et al., where>(1) each one of the directors **having an end user data port *and* an interface state data port, *one of such ports being coupled to a crossbar switch; one of such ports being coupled to a crossbar switch;*** and (2) wherein the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing through the interface state data ports of the directors***.

Claim 55 points out: (1) a plurality of first directors coupled to host computer, each one of the first directors having an ***end user data port*** **and** ***an interface state data port; one of such ports being coupled to a crossbar switch*** and (2) wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.***

It is respectfully requested that the Examiner point out in Hisano et al., where, each one of the first directors having an ***end user data port*** **and** ***an interface state data port; one of such ports being coupled to a crossbar switch; one of such ports being coupled to a crossbar switch*** and (2) wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory ***in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.***

Claim 56 points out that: (1) each one of the directors having an end user data port ***and*** an interface state data port, one of such ports being coupled to a crossbar switch, one of such ports being coupled to a crossbar switch; (2) wherein the directors control end user data transfer with end user data in such end user data transfer passing to the cache memory through the end user data ***ports in response to interface state data passing through the interface state data ports of the directors.***

It is respectfully requested that the Examiner point out in Hisano et al., where: (1) each one of the directors having an end user data port ***and*** an interface state data port, one of such ports being coupled to a crossbar switch, one of such ports being coupled to a crossbar switch; (2) wherein the directors control end user data transfer with end user data in such end user data transfer passing to the cache memory through the end user data ***ports in response to interface state data passing through the interface state data ports of the directors.***

Claim 57 points out: (1) each one of the first directors having an end user data port ***and*** an interface state data port, one of such ports being coupled to a crossbar switch; and (2) wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the end user data ***ports in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors***.

It is respectfully requested that the Examiner point out in Hisano et al., where: (1) each one of the first directors having an end user data port ***and*** an interface state data port, one of such ports being coupled to a crossbar switch; and (2) wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the end user data ***ports in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors***.

Claim 58 points out that: wherein the directors control end user data transfer with end user data in such data transfer passing to the cache memory ***through an end user data communication channel in response to interface state data passing through the directors through a different, interface state data communication channel, one of such channels being coupled to a crossbar switch.***

It is respectfully requested that the Examiner point out in Hisano et al., where: wherein the directors control end user data transfer with end user data in such data transfer passing to the cache memory ***through an end user data communication channel in response***

to interface state data passing through the directors through a different, interface state data communication channel, one of such channels being coupled to a crossbar switch.

Claim 59 points out: wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing ***through an end user communication channel in response to interface state data passing between the first director and the second director through a different, interface state data communication channel one of such channels being coupled to a crossbar switch.***

It is respectfully requested that the Examiner point out in Hisano et al., where: wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing ***through an end user communication channel in response to interface state data passing between the first director and the second director through a different, interface state data communication channel one of such channels being coupled to a crossbar switch.***

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

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Date

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